In the Claims

1. (Currently Amended): A method for collecting statistics in an integrated circuit on data, comprising the steps of:

receiving on an input input data in a first data domain;

converting received input data with a data converter from the first data domain to a second data domain different from the first data domain;

determining with a statistical processor statistical information from the finite collected data from the output of the data converter in the second data domain; ~~and~~

wherein the step of determining operates on a finite amount of collected data from the step of converting;

determining when the completion of the statistical information has occurred; and

allowing ~~external~~ access external to the integrated circuit through an output interface on the integrated circuit to the output of the statistical processor only after the completion of the statistical information.

2. (Currently Amended): The method of Claim 1, wherein the step of converting operates in ~~the time~~ a time domain.

3. (Withdrawn): The method of Claim 1, wherein the step of determining with the statistical processor provides processed statistical output information in the second data domain.

4. (Withdrawn): The method of Claim 1, wherein the step of converting with the data converter operates in the time domain and further comprising the step of receiving the converted data in the second domain from the data converter in the time domain with a time domain/frequency domain converter and converting the received data to frequency domain data in accordance with a predetermined frequency domain conversion algorithm and wherein the step of determining with the statistical processor is operable to obtain statistical information from the output of the time domain/frequency domain converter for processing thereof.

5. (Withdrawn): The method of Claim 4 and further comprising multiplexing with a multiplexer the operation of the step of determining with the statistical processor to select either the output of the data converter or the output of the time domain/frequency domain converter.

6 (Withdrawn): The method of Claim 1 and further comprising storing in memory at least a portion of the processed obtained statistical information.

7. (Withdrawn): The method of Claim 1, wherein:

the step of converting with the data converter is operable to convert the received input data in the first domain to a second domain at a first data width to provide a first amount of data; and

the step of determining with the statistical processor is operable to generate a second and lesser amount of data than the output of the data converter as a result of processing thereby of the obtained statistical information.

8. (Withdrawn): The method of Claim 1, wherein the first domain is an analog data domain and the second domain is a digital data domain.

9. (Withdrawn): The method of Claim 8, wherein the step of converting with the data converter has an output in the digital domain of a first data width and an associated data transfer rate and the output interface has a second data width less than the first data width.

10. (Withdrawn): The method of claim 9, wherein the step of interfacing provides a serial output interface.

11. (Withdrawn): The method of Claim 1 and further comprising the steps of:

providing a dedicated output indicative of information regarding the processing by the step of determining with the statistical processor; and

step of determining with the statistical processor operable to generate an indication for output on the dedicated output.

12. (Withdrawn): The method of Claim 1, wherein the step of converting with the data converter provides samples at a predetermined sample rate and the step of determining with the statistical processor operates on a dataset of the samples as the obtained statistical information.

13. (Withdrawn): The method of Claim 12, wherein the samples in the dataset are adjacent and consecutive.

14. (Withdrawn): The method of Claim 12, wherein the samples in the dataset are quasi-periodic.

15. (Withdrawn): The method of Claim 1, wherein the step of determining with the statistical processor is further operable to process the obtained statistical information in accordance with a predetermined processing algorithm to provide processed statistical information.

16. (Withdrawn): The method of Claim 15, wherein the step of determining with the statistical processor is operable to process the obtained statistical information to determine if the underlying data has an unnatural pattern associated therewith.

17. (Withdrawn): The method of Claim 16, wherein the step of interfacing includes the step of outputting a signal indicative of the presence of an unnatural pattern.

18. (Currently Amended): The method of Claim 1, wherein the step of converting with the data converter provides data at a first sample rate and the step of determining with the statistical processor provides an output at a second ~~data~~ sample rate lower than the first sample rate.

19. (Original): The method of Claim 18, wherein the step of determining with the statistical processor is operable to operate on less than all data samples output by the step of converting with the data converter.

20. (Original): The of Claim 19, wherein the less than all data samples comprises every jth sample, j greater than one.

21. (Withdrawn): The method of Claim 1, wherein the step of converting with the data converter operates in the time domain and further comprising the step o f processing with a post processor to further process the output of the data converter in accordance to a predetermined processing algorithm.

22. (Withdrawn): The method of Claim 21, and further comprising for multiplexing with a multiplexer the operation of the statistical processor to select either the output of the data converter or the output of the post processor.

23. (Withdrawn): The method of Claim 1, wherein the step of determining with the statistical processor includes the step of determining the completion of a statistical operation and the output interface is operable to provide as an output an indication of such completion.

24. (Withdrawn): The method of Claim 23, wherein the step of interfacing is operable to output data and the indication is embedded within the output data as an addendum thereto.

25. (Withdrawn): The method of Claim 23, wherein the completion of the statistical operation comprises determining the presence of an unnatural pattern.

26. (Withdrawn): The method of Claim 1, wherein the step of interfacing allows external access to the output of the data converter.

27. (Currently Amended): An integrated circuit, comprising:

an input for receiving input data in a first data domain;

a data converter for converting received input data from said first data domain to a second domain different from said first domain said data converter collecting data in finite amounts;

a statistical processor for determining statistical information from the output of said data converter, said statistical processor operating on said fixed amounts of data to provide a statistical result on each of said fixed amounts of data; and

an output interface for allowing external access to the output of said statistical processor at the completion of processing of a given one of said fixed amounts of data.

28. (Currently Amended): The integrated circuit of Claim 27, wherein said data converter operates in ~~the time~~ a time domain.

29. (Withdrawn): The integrated circuit of Claim 27, wherein the statistical processor provides processed statistical output information in said second data domain.

30. (Withdrawn): The integrated circuit of Claim 27, wherein said data converter operates in the time domain and further comprising a time domain/frequency domain converter that is operable to receive the converted data in said second domain from said data converter in the time domain and convert the received data to frequency domain data in accordance with a predetermined frequency domain conversion algorithm and wherein said statistical processor is operable to obtain statistical information from the output of said time domain/frequency domain converter for processing thereof.

31. (Withdrawn): The integrated circuit of Claim 30 and further comprising a multiplexer for multiplexing the operation of said statistical processor to select either the output of said data converter or the output of said time domain/frequency domain converter.

32. (Withdrawn): The integrated circuit of Claim 27 and further comprising a memory for storing at least a portion of the processed obtained statistical information.

33. (Withdrawn): The integrated circuit of Claim 27, wherein:

said data converter is operable to convert the received input data in said first domain to a second domain at a first data width to provide a first amount of data; and

said statistical processor is operable to generate a second and lesser amount of data than the output of said data converter as a result of processing thereby of said obtained statistical information.

34. (Withdrawn): The integrated circuit of Claim 27, wherein said first domain is an analog data domain and said second domain is a digital data domain.

35. (Withdrawn): The integrated circuit of Claim 34, wherein said data converter has an output in the digital domain of a first data width and an associated data transfer rate and said output interface has a second data width less than said first data width.

36. (Withdrawn): The integrated circuit of Claim 35, wherein said output interface provides a serial output interface.

37. (Withdrawn): The integrated circuit of Claim 27 and further comprising:

a dedicated output indicative of information regarding the processing by said statistical processor; and

said statistical processor operable to generate an indication for output on said dedicated output.

38. (Withdrawn): The integrated circuit of Claim 27, wherein said data converter provides samples at a predetermined sample rate and said statistical processor operates on a dataset of said samples as said obtained statistical information.

39. (Withdrawn): The integrated circuit of Claim 38, wherein said samples in said dataset are adjacent and consecutive.

40. (Withdrawn): The integrated circuit of Claim 38, wherein said samples in said dataset are quasi-periodic.

41. (Withdrawn): The integrated circuit of Claim 27, wherein said statistical processor is further operable to process said obtained statistical information in accordance with a predetermined processing algorithm to provide processed statistical information.

42. (Withdrawn): The integrated circuit of Claim 41, wherein said statistical processor is operable to process said obtained statistical information to determine if the underlying data has an unnatural pattern associated therewith.

43. (Withdrawn): The integrated circuit of Claim 42, wherein said output interface includes means for outputting a signal indicative of the presence of an unnatural pattern.

44. (Currently Amended): The integrated circuit of Claim ~~27~~, wherein said data converter provides data at a first sample rate and said statistical processor provides an output at a second ~~data~~ sample rate lower than said first sample rate.

45. (Original): The integrated circuit of Claim ~~44~~, wherein said statistical processor is operable to operate on less than all data samples output by said data converter.

46. (Original): The method of Claim ~~45~~, wherein said less than all data samples comprises every jth sample, j greater than one.

47. (Withdrawn): The method of Claim 27, wherein said data converter operates in the time domain and further comprising a post processor for further processing the output of said data converter in accordance to a predetermined processing algorithm.

48. (Withdrawn): The method of Claim 47, and further comprising a multiplexer for multiplexing the operation of said statistical processor to select either the output of said data converter or the output of said post processor.

49. (Withdrawn): The method of Claim 27, wherein said statistical processor includes means for determining the completion of a statistical operation and said output interface is operable to provide as an output an indication of such completion.

50. (Withdrawn): The method of Claim 49, wherein said output interface is operable to output data and said indication is embedded within said output data as an addendum thereto.

51. (Withdrawn): The method of Claim 50, wherein said completion of said statistical operation comprises determining the presence of an unnatural pattern.

52. (Withdrawn): The method of Claim 27, wherein said output interface allows external access to the output of said data converter.